AMENDMENTS TO THE CLAIMS

1. (Currently Amended): An apparatus that measures electrical characteristics of an electrical element within a semiconductor device in a packaged state, comprising;

an electrical characteristic measurer that is connected to the electrical element and a pad of the semiconductor device, ~~and that is~~ said electrical characteristic measurer being driven in response to a control signal to output to the pad a value that is indicative of the electrical characteristics of the electrical element ~~to the pad~~, the control signal being activated in an electrical characteristic measuring mode, after the semiconductor device is packaged,

wherein the pad is not connected to any output driver of the semiconductor device.

2. (Original): The apparatus of claim 1, further comprising a control signal generator that receives at least one bit of an address signal that is received at an address pin of the semiconductor device, and that generates the control signal responsive thereto.

3. (Original): The apparatus of claim 1, wherein the electrical element is selected from a group including an NMOS transistor, a PMOS transistor and a resistor, and the value is indicative of one of a threshold voltage and a saturation

current of the NMOS transistor, one of a threshold voltage and a saturation current of the PMOS transistor, and a resistance of the resistor.

4. (Currently amended): ~~The apparatus of claim 1~~ An apparatus that measures electrical characteristics of an electrical element within a semiconductor device in a packaged state, comprising:

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an electrical characteristic measurer that is connected to the electrical element and a pad of the semiconductor device, and that is driven in response to a control signal to output to the pad a value that is indicative of the electrical characteristics of the electrical element,

the control signal being activated in an electrical characteristic measuring mode, after the semiconductor device is packaged,

wherein the electrical characteristic measurer includes an NMOS transistor having a drain and a source, one of the drain and the source being connected to the pad, and the other of the drain and the source being connected to a terminal of the electrical element, a size of the NMOS transistor being the same as a size of an NMOS transistor connected to a pad of a data input/output pin.

5. (Original): The apparatus of claim 1, wherein the electrical element is a transistor, and the value is indicative of one of a threshold voltage and a saturation current of the transistor.

6. (Original): The apparatus of claim 5, wherein the transistor is an NMOS transistor.

7. (Original): The apparatus of claim 5, wherein the transistor is a PMOS transistor.

8. (Original): The apparatus of claim 1, wherein the electrical element is a resistor, and the value is indicative of a resistance of the resistor.

9. (Currently amended): An apparatus for measuring characteristics of an electrical element within a semiconductor device in a packaged state, comprising:

a control signal generator, coupled to receive an address signal of the semiconductor device, that generates a control signal; and

an electrical characteristic measurer, to which the electrical element is connected, that is driven responsive to the control signal to output to a first pad of the semiconductor device a value indicative of the electrical characteristics of the electrical element,

wherein the first pad is not connected to any output driver of the semiconductor device.

10. (Original): The apparatus of claim 9, wherein the electrical element is one of a transistor and a resistor, the electrical characteristic measurer comprising at least

one transistor characteristic measuring unit that measures the electrical characteristics of the transistor, and a resistor characteristic measuring unit that measures the electrical characteristics of the resistor, as selectable by the control signal.

11. (Original): The apparatus of claim 10, wherein the electrical characteristics of the transistor are one of a threshold voltage and a saturation current.

12. (Original): The apparatus of claim 10, wherein the electrical characteristics of the resistor is a resistance.

13. (Original): The apparatus of claim 10, wherein the control signal generator generates the control signal responsive only to two bits of the address signal.

14. (Original): The apparatus of claim 9, wherein the control signal is generated during an electrical characteristic measuring mode, after the semiconductor device is packaged.

15. (Currently amended): A method of measuring electrical characteristics of an electrical element within a semiconductor device in a packaged state, comprising:

connecting the electrical element of the semiconductor device to an electrical characteristic measurer, after the semiconductor device is packaged;

controlling the semiconductor device to enter into a predetermined electrical characteristic measuring mode;

generating a control signal; and

driving the electrical characteristic measurer responsive to the control signal, to ~~provide~~ output a value indicative of the electrical characteristics of the electrical element to a first pad of the semiconductor device that is not connected to any output driver of the semiconductor device.

16. (Original): The method of claim 15, wherein said controlling comprises:

receiving an address signal provided to an address pin of the semiconductor device; and

entering into a specific sub mode of the electrical characteristic measuring mode responsive to a value of at least one bit of the address signal.

17. (Original): The method of claim 15, wherein the electrical element is selected from a group including an NMOS transistor, a PMOS transistor and a resistor, and wherein the value provided during said driving is indicative of one of a threshold voltage and a saturation current of the NMOS transistor, one of a threshold voltage and a saturation current of the PMOS transistor, and a resistance of the resistor.

18. (New): The apparatus of claim 9, wherein the electrical characteristic measurer includes an NMOS transistor having a drain and a source, one of the drain and the source being connected to the first pad, and the other of the drain and the source being connected to a terminal of the electrical element, a size of the NMOS transistor being the same as a size of an NMOS transistor connected to a second pad that is connected to a data input/output pin,

wherein an output driver of the semiconductor device is connected to the second pad.

19. (New): The method of claim 15, wherein the electrical characteristic measurer includes an NMOS transistor having a drain and a source, one of the drain and the source being connected to the first pad, and the other of the drain and the source being connected to a terminal of the electrical element, a size of the NMOS transistor being the same as a size of an NMOS transistor connected to a second pad that is connected to a data input/output pin,

wherein an output driver of the semiconductor device is connected to the second pad.